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(54) Fingerprint detector with scratch resistant surface and embedded ESD protection grid

(57) A fingerprint detector having a smooth sensor surface for contact with a fingerprint includes capacitive sensor plates defining an array of sensor cells below the sensor surface and tungsten ESD protection grid lines surrounding each sensor cell. The sensor surface is defined by silicon carbide and includes silicon oxide filling cavities in the silicon carbide. The cavities inherently result from processing steps, including removal of the tungsten atop the silicon carbide that is used to define the grid lines. Filling the cavities with oxide and smoothing the surface using chemical mechanical polishing provides a scratch-resistant surface and improves the sensitivity of the capacitive sensor cells.

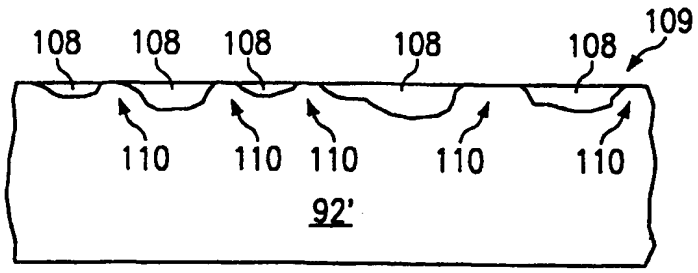

FIG. 11

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Description

[0001] The present invention relates generally to semiconductor fingerprint detectors, and more particularly to improvements in the structure of a fingerprint detection surface used on a fingerprint detector device, and its method of manufacture.

[0002] A capacitive distance sensor is disclosed in commonly-assigned U.S. Patent No. 6,114,862, the disclosure of which is hereby incorporated by reference. The capacitive distance sensor disclosed in this patent is particularly useful in semiconductor fingerprint detectors. The present invention provides an improvement in the structure of the surface that is provided for contact with the fingerprint of the user. Figures 1 and 2 herein correspond to Figures 1 and 4 of U.S. Patent No. 6,114,862, and are briefly described below to facilitate an understanding of the present invention.

[0003] FIG. 1 is a block diagram of a prior art sensor device for which the present invention provides an improvement;

[0004] FIG. 2 is an enlarged schematic side view of a small portion of a finger positioned above two adjacent sensor cells of the device of FIG. 1;

[0005] FIGS. 3-7 are schematic cross sections illustrating a sequence of conventional process steps for making the sensor device of FIG. 1;

[0006] FIG. 8 is an enlarged view of a portion of FIG. 7 showing additional structural details;

[0007] FIG. 9 is a schematic plan view of the layout of the capacitor plates of one sensor cell (overlying insulating layers not shown);

[0008] FIG. 10 is an enlarged plan view of a portion of a tungsten lattice used in the device of FIG. 1;

[0009] FIG. 11 is a greatly enlarged cross section of a top surface portion of an improved sensor device according to the present invention; and

[0010] FIG. 12 is an enlarged cross section of the improved sensor device showing the top layers just prior to the final step of the improved process of the present invention.

[0011] In the cross-sectional views of FIGS. 3-8, 11 and 12, conductive portions are cross-hatched and non-conductive portions are left without cross-hatching for clarity of illustration.

[0012] FIG. 1 shows a sensor device 1 for sensing a distance between the sensor device and an object, such as a finger. The sensor device 1 includes a number of cells 2 arranged to form an array 3 and each constituting an elementary sensor. The simplicity of the individual cells 2 enables the sensor device 1 to be implemented in integrated form on a single semiconductor chip.

[0013] The sensor device 1 also comprises a horizontal scanning stage 5 and a vertical scanning stage 6 for enabling one of the cells 2 at a time according to a predetermined scanning pattern. The stages 5 and 6 enable the outputs of the cells to be read using shift registers, address decoders, or other suitable circuitry.

[0014] The sensor device 1 also composes a supply and logic unit 7, which supplies the circuit elements of the device with power (including the cells 2), feeds the necessary reference voltages, and controls the timing of device operations. FIG. 1 shows that the supply and logic unit 7 includes a voltage source 12. A buffer 8 is interconnected with the outputs of all the cells 2, and includes an output 10 for sequentially generating signals corresponding to the outputs of the cells 2 according to the sequence in which they are enabled by scanning the stages 5, 6.

[0015] FIG. 2 shows the details of two adjacent cells 2A and 2B with a skin surface portion 18 of a human finger positioned thereover. The elements of each of these two cells bear the designators A or B but are essentially identical, as will now be described. Each cell 2 preferably comprises a low-power inverting amplifier 13 having an input 16 and an output 17, which also defines the output of individual cell 2. Each cell 2 also preferably includes first and second coplanar capacitor plates 23 and 24, positioned facing the skin surface 18 of the finger being printed. The plates 23, 24 are covered with a dielectric layer 25 that covers the face of the integrated sensor device 1, including the entire array 3 of cells 2. A reset switch 19 is connected between the input 16 and output 17 of the inverting amplifier 13. An input capacitor 20 is connected between an input 21 of the cell 2 and the input 16 of the inverting amplifier 13. The input 16 of the inverting amplifier 13 also has an equivalent input capacitance depicted by capacitor 30. Likewise, the output 17 has an equivalent output capacitance depicted by capacitor 31.

[0016] The skin surface 18 includes a ridge 39 adjacent to the first cell 2A and a valley 38 adjacent to the second cell 2B. As a result, the first and second cells 2A, 2B will each produce different capacitive coupling responses in the sensor device 1. Accordingly, the first cell 2A will sense a smaller distance d1, signifying the ridge 39, than the second cell 2B, which senses a larger distance d2, signifying the valley 38. The distance d2 sensed by the second cell 2B will be the average of a distance d2a between the first capacitor plate 23B and the portion of the skin surface 18 directly above the first capacitor plate 23B and a distance d2b between the second capacitor plate 24B and the portion of the skin surface 18 directly above the second capacitor plate 24B. From a lumped-model point of view, this structure realizes a three-capacitor scheme that can sense the difference between a contacting member, a ridge, and a non-contacting member, a valley.

[0017] It will be appreciated that the durability of the top surface of the dielectric layer 25 is an important concern. The prior art device just described was provided with a thin silicon carbide layer on the upper surface. The final steps in the sequence of processing steps are illustrated in FIGS. 3-8, and will now be described briefly to highlight the improvement made by the present invention hereinafter disclosed.

[0018] FIG. 3 schematically illustrates one capacitive sensor cell and other common structures within the device. The device is fabricated on a conventional monocrystalline silicon substrate 50, the upper layer of which may be epitaxially formed. Relatively thick field oxide layers 52 and 54 define an active area 56 therebetween. The active area 56 is typical of many such active areas repeated throughout the device, which may include N-type or P-type regions (not shown) of conventional transistor elements.

[0019] The gate structure of a typical transistor is shown immediately above the active area 56, and includes a polysilicon gate 58, a thin gate oxide layer 60, and sidewall oxide spacers 62. Polysilicon interconnects 64, which are shown atop the field oxide layers 52 and 54, are used to interconnect other transistor elements (not shown) of the device.

[0020] Overlying the polysilicon gate 58 and polysilicon interconnects 64 is a relatively thick dielectric layer 66, which is preferably a doped oxide such as borophosphosilicate glass (BPSG). A first metalization layer defines metal interconnects 68 and vias 70 extending down through the BPSG layer 66 to contact the polysilicon gate 58 and polysilicon interconnects 64. Preferably, the metal used to define the interconnects 68 and vias 70 is primarily aluminum with traces of silicon (about 1.0%) and copper (about 0.5%). A very thin composite layer (not shown) of titanium and titanium nitride is interposed at each interface between each via 70 and the polysilicon material therebelow.

[0021] A planarized dielectric layer 72 covers the metal interconnects 68 and BPSG layer 66. Preferably, dielectric layer 72 is a composite of a lower undoped oxide, an intermediate spin-on-glass (SOG), and an upper undoped oxide. The lower undoped oxide is first deposited to a thickness of about 5500Å, then the SOG is deposited to a thickness of about 6000Å and etched back to provide a planarized surface, and then the upper undoped oxide is deposited to a thickness of about 5000Å. Next, vias openings are etched through the dielectric layer 72 and a second metalization step is performed. Then, the metal is patterned to define capacitor plates 76 and 78, a ground line 80, and vias 82 down to the interconnects 68. A further dielectric layer 74, preferably of hydrogen silsesquioxane (HSQ), is then deposited atop the SOG layer 72 between the metal plates 76 and 78 and the ground line 80.

[0022] The second metalization layer is preferably of the same primarily aluminum composition as the first metalization that defines the interconnects 68. The ground line 80 is connected to a ground pad (not shown) at the periphery of the semiconductor chip. The portion of the chip that includes the metal ground line 80 is shown broken away since it is actually located beyond the periphery of the array of capacitive sensor cells. Two additional dielectric layers are deposited atop the HSQ layer 74 and the portions of the second metalization layer embedded therein. These two additional dielectric layers preferably comprise a phosphosilicate glass (PSG) layer 84 and a silicon nitride ($Si_x N_y$) layer 86.

[0023] Now referring to FIG. 4, the fabrication process continues with the formation of a third metalization layer. Plug openings are etched through the dielectric layers 84 and 86 down to the aluminum ground line 80. A very thin film (not shown) of titanium nitride (TiN) is conformally deposited on the silicon nitride layer 86, on the walls within the plug openings through layers 84 and 86, and on the surface of the aluminum ground line 80 exposed inside the plug openings. Next, a tungsten (W) layer 88 is conformally deposited on the very thin titanium nitride film above the silicon nitride layer 86 and within the plug openings above the ground line 80.

[0024] Now referring to FIG. 5, the structure is shown after etching back the tungsten layer 88 and underlying titanium nitride down to the surface of the silicon nitride layer 86. This leaves tungsten plugs 90 in place, which are electrically connected to the aluminum layer 80 through the very thin titanium nitride film. The surface of the silicon nitride layer 86 is left in a relatively rough state since the tungsten layer 88 (FIG. 4) has a strong columnar structure and etches back unevenly, the fastest etching occurring along grain boundaries. The roughness is transferred to the underlying titanium nitride film (not shown) and then to the silicon nitride layer 86 upon dry-etch removal of the titanium nitride.

[0025] As previously mentioned, the aluminum layer 80 is connected to a ground pad (not shown), which is located at the periphery of the device. The purpose of the tungsten plugs 90 is to provide an electrostatic discharge (ESD) path to ground from the top surface of the device when touched by an object, such as a human finger. The aluminum layer 80 is provided in a peripheral pattern, preferably along two or three sides of the array of sensor cells, with thousands of tungsten plugs 90 juxtaposed thereover.

[0026] FIG. 6 shows the structure after several additional steps have been performed. A silicon carbide layer 92 is deposited on the silicon nitride layer 86 and atop the tungsten plugs 90. Some of the roughness of the silicon nitride layer 86 appears at the top surface of the silicon carbide layer 92. Then, the silicon carbide is patterned, using conventional photolithographic techniques, to open spaces around each sensor cell and over the tungsten plugs 90. Another thin film (not shown) of titanium nitride is conformally deposited on the silicon carbide layer 92 and within the spaces opened therethrough. Next, an additional tungsten metalization step is performed to provide tungsten layer 94 as shown.

[0027] Next, with reference to FIG. 7, the tungsten layer 94 is etched back leaving tungsten grid lines 96 and a tungsten peripheral line 98 in place. Then, the titanium nitride film (not shown) is removed from the silicon carbide layer 92. The inherent roughness of the tungsten layer 94 is transferred through to the silicon carbide layer 92 upon removal by dry etching of the tungsten layer 94 and underlying titanium nitride film. The result leaves

the silicon carbide layer 92 with a rough top surface 100.

[0028] FIG. 8 is an enlarged view of a portion of FIG. 7 showing the tungsten line 98 and its connection to the aluminum ground line 8 through intermediate conductive structures. Shown greatly exaggerated in thickness are titanium nitride films 102 and 104, which were mentioned above but not shown in the previous figures.

[0029] FIG. 9 shows the preferred layout of one capacitive sensor cell 2, which includes separate capacitor plates 76 and 78. The first capacitor plate 76 is C-shaped and the second capacitor plate 78 has portions within and outside of the C-shaped first plate 76. Tungsten grid lines 96 are shown surrounding the sensor cell 2. This pattern is repeated throughout the array 3 of cells described above with reference to FIG. 1. For simplicity of illustration, the grid lines 96 are shown as single lines forming a square around the sensor cell 2 of FIG. 9. Preferably, however, the grid lines 96 are actually more complex in their layout, as will now be described.

[0030] FIG. 10 shows an enlarged plan view of a portion of a grid line 96 and a portion of a peripheral line 98, each of which is laid out as a lattice or network of diagonally crossing microlines 106. Each microline 106 is approximately one micron in width. Within the lattice of the peripheral line 98 and therebelow are the previously mentioned tungsten plugs 90, which are depicted schematically as circles at spaced intersections of selected microlines 106. A plurality of parallel rows of tungsten plugs 90 are used, two being shown, but as many as five rows of staggered plugs being employed in practice.

[0031] The process steps described above are well known in the art of semiconductor fabrication. The resulting structures described above are also in the prior art and have been in use in commercial products for more than one year before the filing of this application. The invention described below provides an improvement in the fabrication of fingerprint detectors and in their reliability and performance.

[0032] It has been discovered that the rough surface of the silicon carbide layer used in prior art fingerprint detectors is capable of being damaged by scratching with fingernails or other relatively hard objects. A method has been devised to provide a smooth surface that resists scratching. The method steps include depositing an oxide layer on the surface of the device to fill cavities in the rough surface of the silicon carbide layer, and then removing most of the deposited oxide by chemical mechanical polishing. This leaves a smooth surface with oxide filling the cavities between high points of the silicon carbide surface.

[0033] In accordance with the present invention, the durability and reliability of the above-described fingerprint detector is improved by additional processing, as described below. FIG. 11 is a greatly enlarged view of a portion of silicon carbide layer 92', which is similar to previously described silicon carbide layer 92 of FIG. 7. Added to the previously described structure are silicon oxide fillings 108 that fill in cavities in the rough top surface of silicon carbide layer 92'. The cavities are very small, typically having a maximum lateral dimension of about 150Å and a maximum depth of about 100Å. The resulting structure has a smooth top surface 109 consisting of silicon carbide at random high points 110 and silicon oxide fillings 108 in the cavities therebetween.

[0034] The preferred method of producing the smooth top surface 109 proceeds with the method steps described above in connection with FIGS. 3-8 with the following additional steps. A silicon oxide layer 112 is deposited on the rough top surface 100' of the silicon carbide layer 92' to produce the structure shown in the enlarged partial view of FIG. 12. Preferably, the oxide layer 112 is at least about 250Å, which is more than adequate to fill the cavities in the top surface of the silicon carbide layer 92'. A conventional chemical vapor deposition (CVD) process is used to deposit the oxide layer 112. This is performed at a relatively low temperature between 360°C and 400°C, preferably at about 380°C.

[0035] Then, using chemical mechanical polishing (CMP), most of silicon oxide layer 112 is removed to produce the structure that is partially shown in the greatly enlarged view of FIG. 11. In practice the thickness of oxide layer 112 will be determined by the requirements of the CMP procedure, which may need to operate for a minimum time for consistent results. The preferred slurry used in this CMP step is Klebosol®, which can be purchased from Rodel, Inc. of Phoenix, Arizona.

[0036] It will be appreciated from the foregoing description that the addition of oxide fillings 108 in the cavities greatly improves the ability of the device to resist damage from scratching. The cavities themselves are much smaller than the dimensions of the edge of a fingernail or other object that typically might contact the sensor surface 109. Thus, the oxide will stay lodged in the cavities and will present a smooth, scratch-resistant surface to the user.

[0037] Additionally, it will be appreciated that the sensitivity of the capacitive difference measurements will improve with the inclusion of the oxide fillings 108 in the cavities in the top surface of the silicon carbide layer 92' due to the change in the dielectric composition of the capacitors. In other words, removal of the air volumes of the cavities between the sensor surface and the ridges and valleys of a fingerprint of a user will increase the capacitance values and the ability to detect small differences in capacitance measurements.

[0038] Although the preferred embodiment has been described in detail, it should be understood that various changes, substitutions and alterations can be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. A fingerprint detector device comprising:

a semiconductor substrate;
an array of capacitive sensor cells formed on the semiconductor substrate;
a tungsten grid having grid lines surrounding each sensor cell and having a peripheral ground line;
a silicon carbide layer disposed above the sensor cells, the tungsten grid being embedded in the silicon carbide layer and having exposed surface portions for contacting a fingerprint pressed against the detector device, the silicon carbide layer including cavities at the top surface; and
silicon oxide fillings filling in the cavities in the top surface of the silicon carbide layer, the silicon oxide fillings and silicon carbide layer providing a smooth top surface for the device.

2. The fingerprint detector of Claim 1 wherein the silicon carbide layer is part of a stacked arrangement of dielectric layers supported by the simiconductor substrate, and wherein the capacitive sensor cells include metal capacitor plates embedded in an intermediate dielectric layer of the stacked arrangement.

3. The fingerprint detector of Claim 2 wherein the metal capacitor plates of each capacitive sensor cell are two in number and are coplanar.

4. The fingerprint detector of Claim 3 wherein the one of the two metal capacitor plates of each sensor cell is generally C-shaped and the other of the two metal capacitor plates has portions within and outside of the C-shaped plate.

5. The fingerprint detector of Claim 4 wherein the metal capacitor plates each consists essentially of aluminum.

6. A method of making a fingerprint detector comprising:

providing a semiconductor substrate with transistor regions defined therein;
forming conductive layers above the substrate to interconnect the transistors;
forming a planarized insulating layer above the conductive layers;
defining coplanar capacitor plates on the planarized insulating layer with vias through the planarized insulating layer to portions of the conductive layers therebelow;
depositing a silicon carbide layer above and insulated from the capacitor plates;
defining openings within the silicon carbide layer;
depositing a titanium nitride film on the silicon carbide layer and within the openings therein;
depositing a tungsten layer on the titanium nitride layer;
selectively etching back the tungsten layer to remove the tungsten except within the openings;
removing the titanium nitride above the surface of the silicon carbide layer leaving cavities in the top surface of the silicon carbide layer;
depositing a thin oxide layer on the silicon carbide layer and within the cavities; and
removing portions of the thin oxide layer by chemical mechanical polishing down to high points of the silicon carbide layer and leaving oxide in the cavities so that the remaining oxide and high points of the silicon carbide layer define a smooth surface for contact by a fingerprint of a finger.

7. The method of Claim 6 wherein the thin oxide layer is deposited by chemical vapor deposition at a temperature of between about 360°C to about 400°C.

8. The method of Claim 7 wherein the thin oxide layer is deposited to a thickness above the silicon carbide layer of at least about 250Å.

9. The method of Claim 6 wherein tungsten plugs are formed beneath the tungsten layer within the openings to provide connection to a metal ground line therebelow.

10. The method of Claim 9 wherein the capacitor plates are formed by depositing a metal layer and selectively removing portions of the metal layer to define the capacitor plates and the metal ground line during the same sequence of steps.

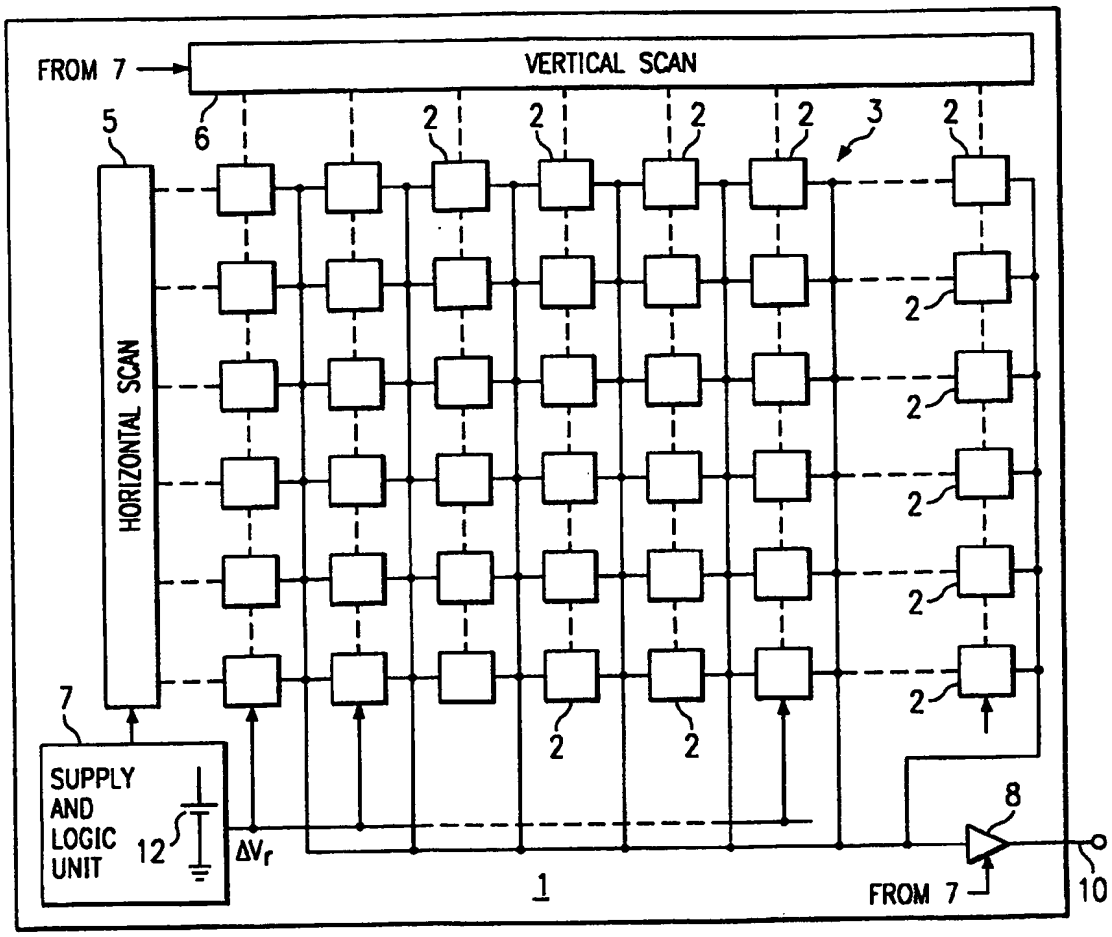


FIG. 1
(PRIOR ART)

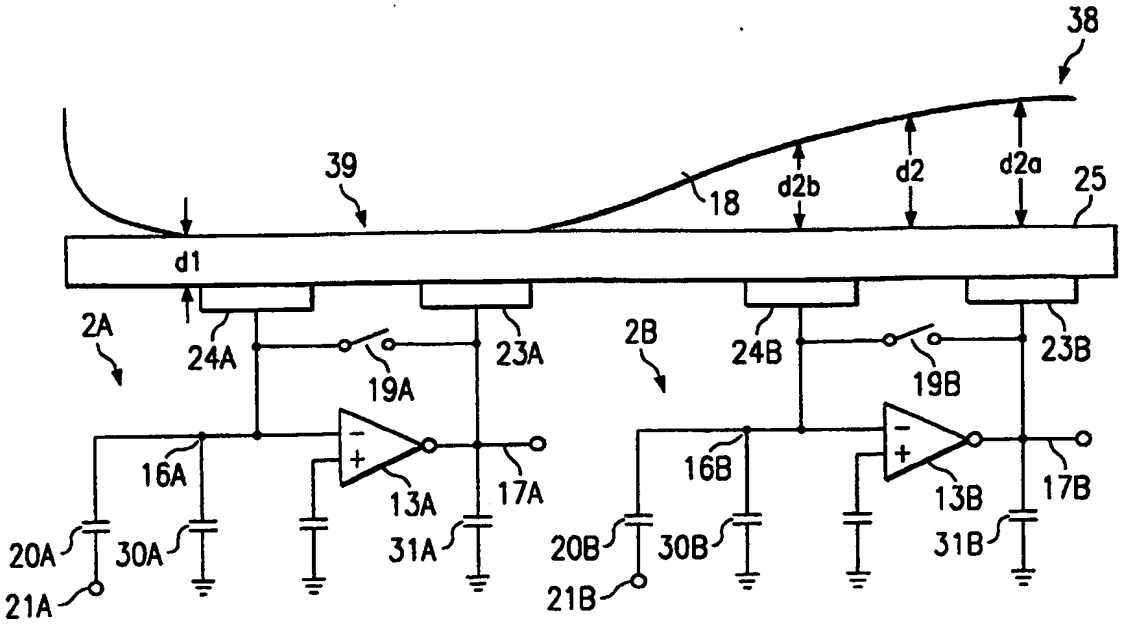


FIG. 2
(PRIOR ART)

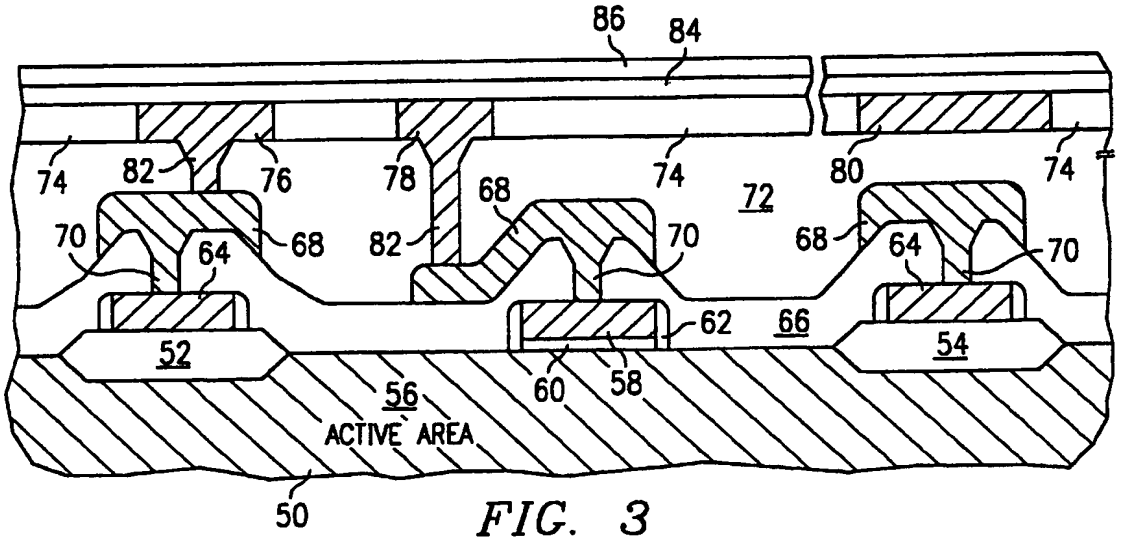


FIG. 3
(PRIOR ART)

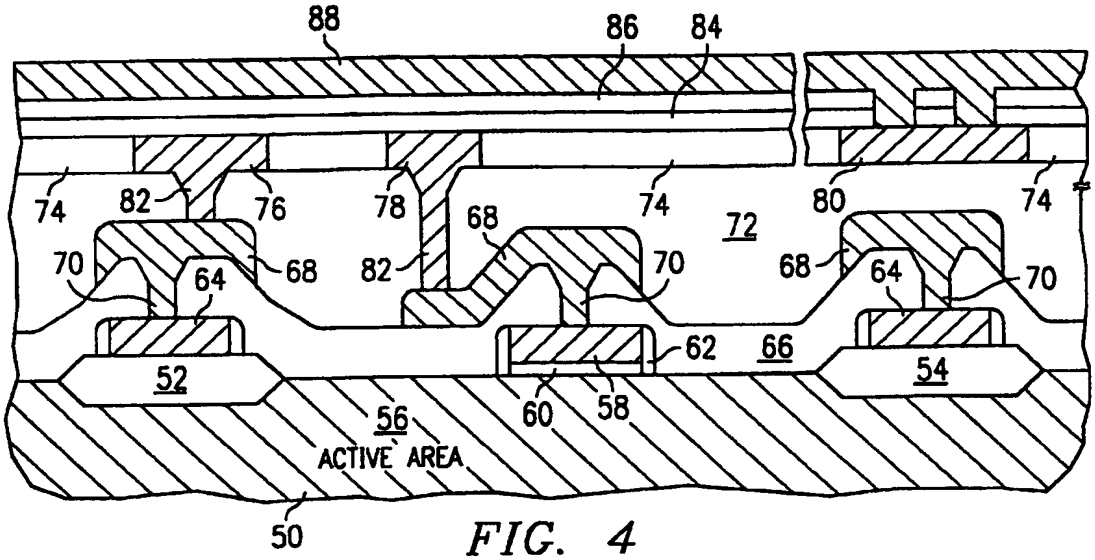


FIG. 4
(PRIOR ART)

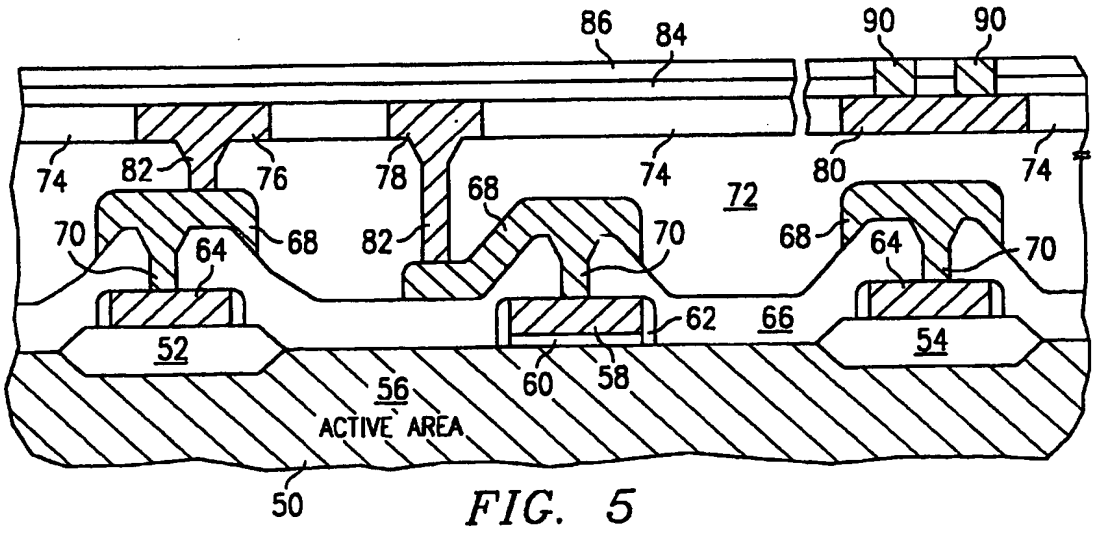


FIG. 5
(PRIOR ART)

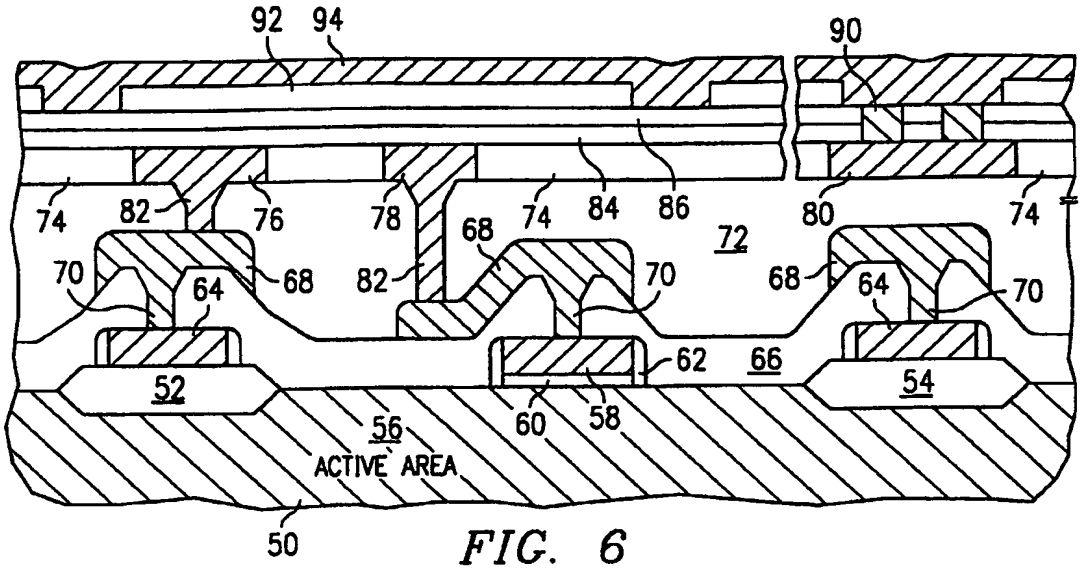


FIG. 6
(PRIOR ART)

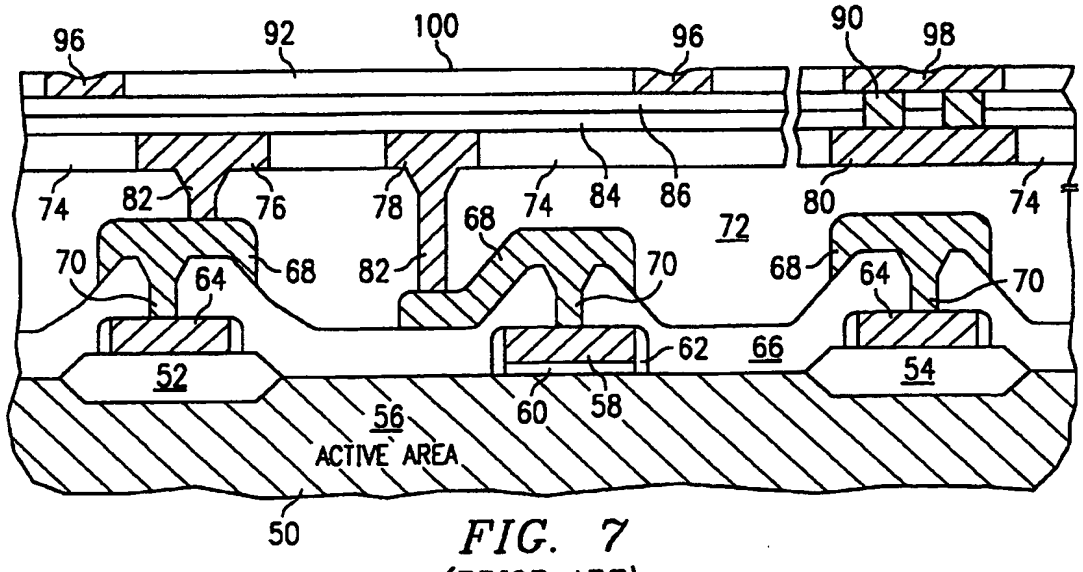


FIG. 7
(PRIOR ART)

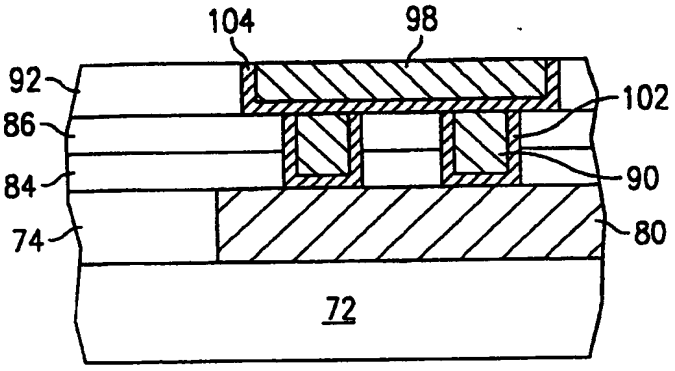


FIG. 8
(PRIOR ART)

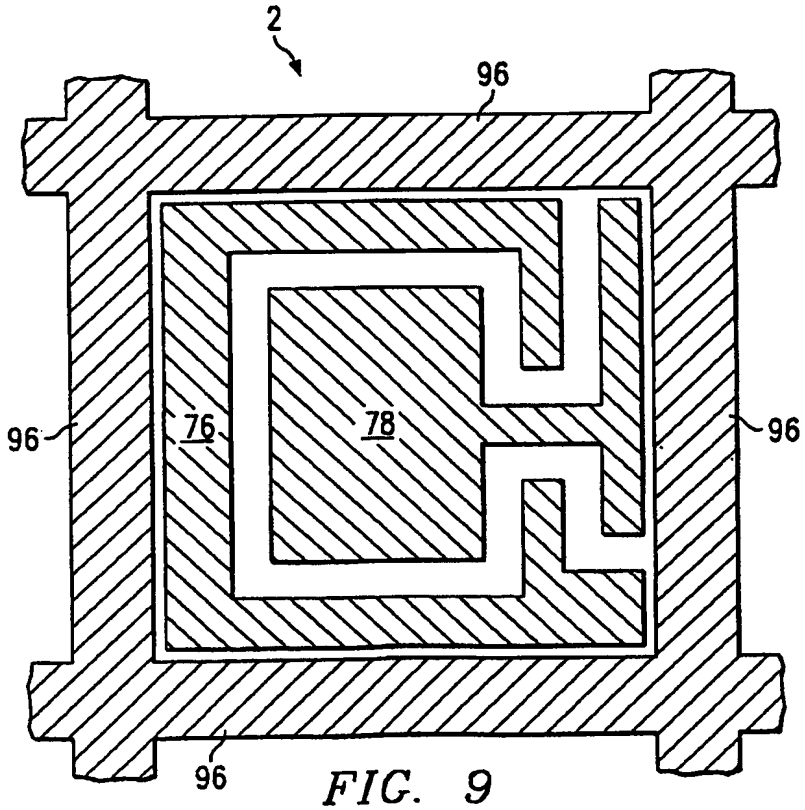
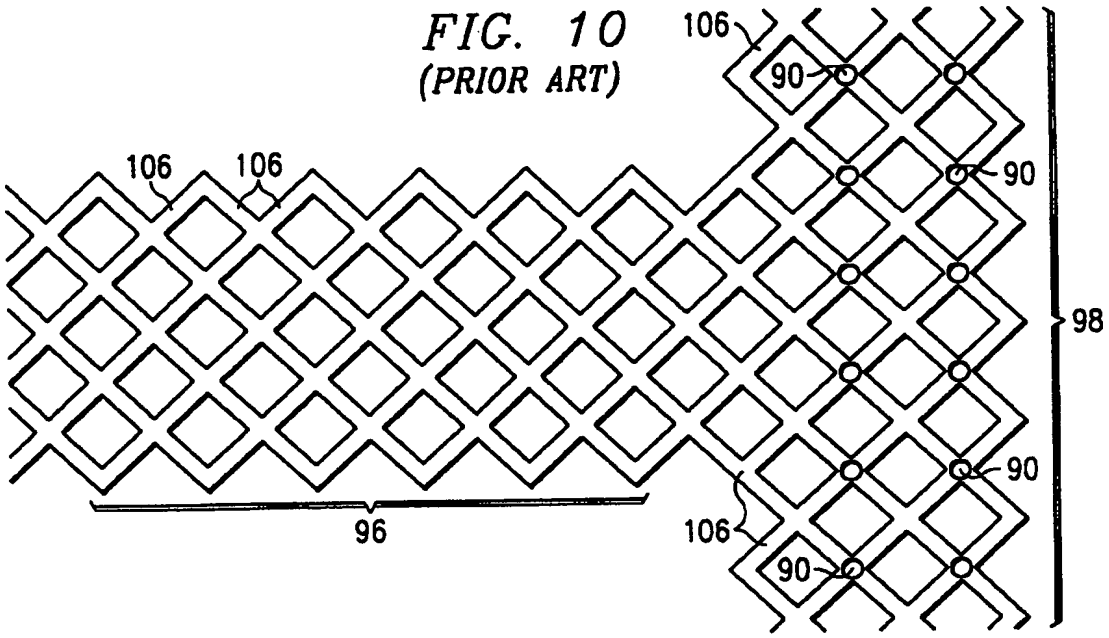


FIG. 9
(PRIOR ART)

FIG. 10
(PRIOR ART)



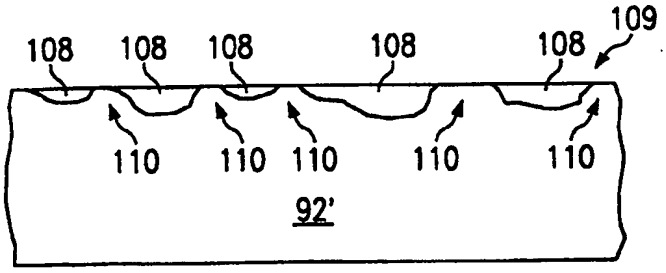


FIG. 11

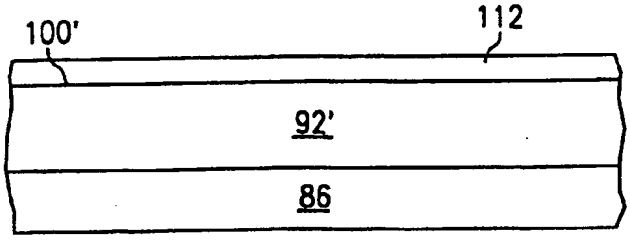


FIG. 12

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 3138

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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A	US 5 801 095 A (HUANG RICHARD J ET AL) 1 September 1998 (1998-09-01) * abstract * * column 4, line 1 - line 14; figures 1A,1B *	6	
A	WO 00 42657 A (GOELLNER REINHARD ;VON BASSE PAUL WERNER (DE); MELZL MICHAEL (DE);) 20 July 2000 (2000-07-20) * claims 1,4; figures 1-3 *	1-3,6,10	
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)
G06K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 August 2002	Granger, B

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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EUROPEAN SEARCH REPORT

Application Number
EP 02 25 3138

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	VERIDICOM: "FPS2000 Silicon Fingerprint Sensor" VERIDICOM CATALOGUE OF SOLUTIONS, [Online] August 2000 (2000-08), pages 1-2, XP002208516 Retrieved from the Internet: <URL:http://www.veridicom.com/products/pdf/fps200_5.15.02.pdf> [retrieved on 2002-08-02] * page 1, right-hand column, paragraph 1 * * page 2 right column, Section "key features and benefits", fourth bullet * -----	1-10	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 August 2002	Granger, B

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O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 25 3138

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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